What is claimed is:

1. An after-package voltage trim circuit for an integrated circuit (IC) for generating a trim voltage signal to add to an initial voltage reference signal generated by said IC, said voltage trim circuit comprising:

an after-package trim cell circuit array configured to receive a sequential binary signal and provide a trim cell circuit array digital signal equal to said sequential binary signal;

a digital to analog converter (DAC) configured to receive said trim cell circuit array digital signal and provide an analog trim current signal representative of said trim cell circuit array digital signal; and

a resistive element configured to convert said analog trim current signal into said trim voltage signal, wherein said trim voltage signal is added to said initial voltage reference signal.

2. The trim circuit of claim 1, wherein said resistive element comprises a resistor.

3. The trim circuit of claim 1, further comprising:

a register configured to provide said sequential binary signal.

4. The trim circuit of claim 3, further comprising an isolation trim circuit configured to isolate said after-package trim cell circuit array from said register upon receiving an isolation signal from said register.

5. The trim circuit of claim 1, wherein said after-package trim cell circuit array comprises a plurality of after-package trim cell circuits.

6. The trim circuit of claim 5, wherein one of said plurality of after-package trim cell circuits includes a sign cell circuit configured to provide a bit value to said DAC representative of a desired sign of said trim current signal.

7. The trim circuit of claim 5, wherein said sequential binary signal has a predetermined number of bits and wherein each of said plurality of after-package trim cell circuits is configured to receive one bit of each of said predetermined number of bits.

8. The trim circuit of claim 7, wherein each one of said plurality of trim cell circuits comprises:

at least one switch responsive to said one bit to conduct when said one bit is high and to not conduct when said one bit is low.

9. The trim circuit of claim 8, wherein each one of said plurality of trim cell circuits further comprises a logic decision circuit having an output coupled to said DAC, wherein said output of said logic decision circuit is high if said at least one switch is conducting and is low if said at least one switch is not conducting.

10. The trim circuit of claim 9, wherein said logic decision circuit comprises an OR gate.

11. The trim circuit of claim 3, further comprising a bus controller configured to control said register to generate said sequential bit signal.

12. A method of trimming a reference voltage for an integrated circuit (IC), said method comprising the steps of:

generating a binary signal sequence;

generating a trim current representative of said binary signal sequence at an output terminal;

generating a trim voltage from a resistive element coupled to said output terminal;

adding said trim voltage to said reference voltage to obtain a sum;

determining if said sum is within a predetermined range of a high precision reference signal; and

fixing said trim voltage if said sum is within said predetermined range.

13. The method of claim 12, wherein said resistive element comprises a resistor.

14. The method of claim 12, wherein said fixing step further comprises permanently setting said binary signal sequence at a value that generates said trim voltage resulting in said sum within said predetermined range.

15. The method of claim 12, wherein said generating said binary signal sequence step comprises controlling a plurality of after-market trim cells to generate said binary signal sequence.

16. The method of claim 14, further comprising the step of isolating said trim cells from said IC after said fixing step.